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[Title of the Invention]

Thin Film Transistor, its Method of Manufacturing and Crystal Display Device


[Abstract]

[Problem]

In a top gate n-type TFT, by obtaining an LDD region with high precision easily, present invention aims to prevent decrease or a variation in TFT mobility, and further, variation in a threshold level to obtain TFT with high mobility and a stable characteristic. Moreover, present invention aims to enhance visual quality of a crystal display device and be applied to large sized crystal display devices.

[Means for Solving the Problem]

By using a gate wiring layer 28, in which a first layer 28a and a second layer 28b are formed into a forward tapered shape and an inverse tapered shape respectively, as a mask, by one time of ion doping process, an LDD region 26-2, a source region 26-3 and a drain region 26-4 are formed to obtain a TFT having a desired length in a self-aligning manner on a semiconductor layer 26.

[Scope of Claims]

[Claim 1]

A thin film transistor device characterized by having:

an insulating substrate;

a channel region composed of a polysilicon that is formed on the insulating substrate;

a source drain region formed by sandwiching said channel region in between through a low concentration impurity region and making said polysilicon low resistive;

a gate-wiring layer which is formed on said channel region through a gate insulating film, having two-layer structure in which a cross-section of channel region side first layer tapered forwardly and a cross section of surface side second layer tapered inversely; and

a source drain-wiring layer connected to said source drain region through an interlayer insulating film

[Claim 2]

The thin film transistor device described in Claim 1 characterized by using an alloy of molybdenum (Mo) for a gate-wiring layer

[Claim 3]

The thin film transistor described in either one of Claim 1 or 2 characterized by the value of c>a>b when a wiring line width of an interlayer with a gate insulating film in a first layer of a gate wiring line

layer is set to a $\mu$m, a wiring line width of an interlayer in first and second layers is set to b $\mu$m, and a wiring line width of an interlayer in top face of the second layer is set to c $\mu$m

[Claim 4]

The thin film transistor device described in Claim 3 characterized by the value of $0.2\,\mu m \leqq (c-a) \geqq 2\,\mu m$

[Claim 5]

A method of manufacturing a thin film transistor device characterized by having:

a step of forming a polysilicon and a gate insulating film on an insulating substrate;

a step of forming a first gate metal film on said gate insulating film;

a step of forming a second gate metal film on said first gate metal film;

a step of forming two-layer structure gate wiring line layer by processing a cross-section of said first gate metal film into a forward tapered shape and processing a cross-section of said second gate metal film into an inverse tapered shape; and

a step of forming a low concentration impurity region and a source drain region simultaneously by doping ion on said polysilicon layer using the gate wiring line layer as a mask

[Claim 6]

A method of manufacturing the thin film transistor device described in Claim 5 characterized by using an alloy of Molybdenum (Mo) for first and second gate metal films

[Claim 7]

A crystal display device characterized by having:

a first insulating film;

a pixel electrode arranged in matrix on said first insulating substrate;

a channel region composed of a polysilicon formed in said first insulating film;

a source drain region formed by sandwiching said channel region in between and making said polysilicon low resistive;

a gate-wiring layer which is formed on said channel region through a gate insulating film, having two-layer structure in which a cross-section of channel region side first layer tapered forwardly and a cross section of surface side second layer tapered inversely; further,

an array substrate having a source drain-wiring layer connected to said source drain region through an interlayer insulating film and a thin film transistor device driving said pixel electrode;

a counter substrate which has a second insulating film and a counter electrode formed on a second insulating film, arranged opposing to the array substrate; and

a crystalline composition of matter encapsulated between the array substrate and the counter substrate

[Detailed Description of the Invention]

[0001]

[Technical Field to which the Invention Pertains]

Present invention relates to a method of manufacturing a thin film transistor device of top gate type which has a gate wiring line layer above a semiconductor layer through a gate insulating film and a thin film transistor device, and also relates to an active matrix type crystal display device having a top gate type thin film transistor device as a driving element.

[0002]

[Prior Art]

A thin film transistor device (hereafter referred to as TFT) using polysilicon as a semiconductor material is used as a driving element of a pixel portion in an active matrix type crystal display device and a driving element of circuit portion because of the thin TFT's high mobility as tens to hundreds square centimeter. Then, as for an n-type polysilicon TFT of a top gate type generally used as a driving element, a decrease of a leakage current is reduced by providing a low concentration impurity region between a channel region and a drain region of high concentration impurity and by providing low concentration impurity (hereafter referred to as LDD) adding a trace of impurity so as to relief the electric filed applied between a source and a drain because leakage current is occurred when the TFT is off.

[0003]

So far, the TFT having thus LDD region has been manufactured in the manner shown in Fig. 5. That is, ① as Fig. 5 (a) shows, after forming an under coat film 2 composed of silicon oxide ($SiO_2$) on a glass substrate 1 is formed, an amorphous silicon film is laminated, the amorphous silicon film is crystallized into a polysilicon film and patterned in matrix by a leaser annealing, and then a semiconductor layer 3 composed of a polysilicon is formed.

[0004]

② As Fig.5 (b) shows, gate wiring lines 4 and 6 are formed, and an LDD region 3-2 is formed by doping a phosphor ($P^+$) ion with low dose.

[0005]

③ As Fig.5 (c) shows, a resist mask 7 is formed, a phosphor ($P^+$) ion with high dose is doped, and a source drain region 3-3 of n+ is formed on a semiconductor layer 3.

[0006]

④ As Fig. 5 (d) shows, a mask 7 is removed and an interlayer insulating film 8 is formed.

[0007]

⑤ As Fig. 5 (e) shows, contact holes 10a and 10b formed, a source electrode 12 and drain electrode 13 are formed to complete a TFT 14 device having an LDD region.

[0008]

[Problem to be Solved by the Invention]

However, the existing TFT above forms an LDD region using a resist mask, so following problems has been occurred: a length of the LDD region can be controlled only in a range from 1 to 5 $\mu$m by a displacement in pattern when a resist mask is formed and a variation in an amount of side-etching; a subtle control in a range no more than 1 $\mu$m is impossible; variation in the length of the LDD region becomes longer; consequently; a variation in the TFT characteristic is occurred; and on the other hand, the LDD falls into a state of having serial resistance if the length of the LDD region becomes longer, that leads a decrease in a mobility; the pixel is partially visible in a crystal display device; a visual quality is remarkably decreased; and an application to especially a large type active matrix becomes impossible.

[0009]

Then, present invention removes the problems above, makes subtle control in the length of the LDD region possible and has a stable characteristic. Also, present invention aims to provide TFT device realize good visual quality even if it is in a large type active matrix crystal display device, and to provide a manufacturing method of the TFT device and the crystal display device.

[0010]

[Means for Solving the Problem]

Present invention provides an insulating substrate, a channel region comprise by a polysilicon, a source drain region formed by sandwiching the channel region in between through a low concentration impurity region and making said polysilicon low resistive, a gate-wiring layer which is formed on said channel region through a gate insulating film, having two-layer structure in which a cross-section of a channel region side first layer are tapered forwardly and a cross section of surface side second layer are tapered inversely, and a source drain-wiring layer connected to the source drain region through an interlayer insulating film and a source drain-wiring layer connected to the source drain region through an interlayer insulating film to solve the problems above.

[0011]

To solve the problems above, present invention implements steps of forming a polysilicon layer and a gate insulating film on an insulating substrate, forming a first gate metal film on said insulating substrate, forming a second gate metal film on the first gate metal film, forming two-layered structure gate wiring layer by processing the cross-section of said first gate metal film into forwardly tapered and by processing the cross-section of said second insulating film into inversely tapered and forming a low concentration region and a source drain region simultaneously after conducting ion doping in the polysilicon layer.

[0012]

Present invention provides a first insulating substrate, a pixel electrode arranged in matrix on the first insulating substrate, a channel region composed of a polysilicon formed on said first insulating substrate, a source drain region formed by sandwiching said channel region in between through a low concentration impurity region and making said polysilicon low resistive, a gate-wiring layer which is formed on said channel region through the gate insulating film, a gate-wiring layer formed to have two-structure layer in which the cross section of the channel region side first layer are tapered forwardly and the cross section of the surface side second layer are tapered inversely on said channel region through the gate insulating film, a source drain wiring layer connected to said source drain region through an interlayer insulating film,

an array substrate having a thin film transistor device driving the pixel electrode, a second insulating substrate, a counter substrate which has a second insulating film and a counter electrode formed on a second insulating film, arranged opposing to the array substrate and a crystalline composition of matter encapsulated between said array substrate and said counter substrate.

[0013]

By the structure above, the present invention makes it possible to obtain desired LDD length easily and to obtain a crystal display device with good visual quality without occurring the a decrease of TFT mobility and, at the same time, aims a stabilization in TFT characteristic.

[0014]

[Embodiment Mode of the Invention]

With the reference of Fig.1 to Fig. 3, embodiment modes of the present invention are to be described in the following. A number 16 denotes an active matrix crystal display device, and it has a crystalline composition of matter 21 and also polarizing plates 22a and 20b between an array substrate 18 and a counter substrate 19 through orientation films 20a and 20b. The array substrate has a top gate type TFT 17 containing a poly silicon semiconductor layer as a driving element.

[0015]

Here, on an undercoat layer 24 composed of a silicon oxide ($SiO_2$) on a glass substrate 23 that is a first insulating substrate of the array substrate 18, a channel region 26-1 formed of a poly silicon, an LDD region 26-2 doped with low dose phosphor ($P^+$) ion, source region 26-3 doped with high dose phosphor ($P^+$) ion, an n type semiconductor layer 26 having a drain region 26-4 are patterned. In addition, on this semiconductor 26, though a gate insulating film 27, TFT 17 having a gate-wiring layer 28 comprised of two-layered structure Molybdenum –Tungsten alloy (hereafter referred to as MoW) is provided. The two-layered structure is composed of a cross section of a first layer 28a, a first gate metal film, which is forwardly tapered at an angle of 30° and a cross section of a second layer 28b, a second gate metal film, which is inversely tapered at an angle of 30° . Moreover, on a same surface with the gate wiring line layer 28, an auxiliary capacitor line 30 is formed.

[0016]

Further, though an interlayer insulating film 31, a pixel electrode 32 is formed, and a drain electrode 33 integrated with a signal line, a source electrode 34 connecting to the source region 26-3 and the pixel electrode 32 are formed on the interlayer insulating film 31. The drain electrode and the source electrode are respectively connected to the drain region 26-4,

the source region 26-3. Incidentally, a number 36 denotes a protective film.

[0017]

On the other hand, a counter substrate 19 has a counter electrode 38 and a protective film 40 in the whole area of a glass substrate, injects a crystalline composition of matter 21 between the counter substrate and the array substrate, and forms a crystal display device 16.

[0018]

A process of manufacturing the TFT 17 on the array substrate 18 will be given next.

[0019]

① As shown in Fig. 3 (a), on a glass substrate 23, the under coat layer 24 composed of a silicon oxide ($SiO_2$) and an amorphous silicon film 41 are layered sequentially. By laser annealing, the amorphous silicon film 41 is crystallized into a poly silicon film.

[0020]

② A shown in Fig. 3 (b), a semiconductor layer26 compose of a crystallized poly silicon is patterned in matrix.

[0021]

③ As shown in Fig. 3 (c), after a gate insulating film is formed to have thickness of 100nm, the first layer 28a of the gate wiring line layer 28, is formed to have a thickness of 50nm with MoW by sputtering and is exposed to an atmospheric air

[0022]

④ As shown in Fig. 3 (d), after the second layer 28b of the gate wiring line layer 28 is formed to have thickness of 35nm by sputtering, the first layer 28a is processed into forwardly tapered shape to have 5 $\mu$m in a wiring width a of an interface with the gate insulating film 27 and 4.8 $\mu$m in a wiring width b of an interface with the second insulting film 28b by an isotropic dry etching. The second layer 28b of the gate wiring line layer 28 processed into inversely tapered to have 6.2 $\mu$m in a wiring width c in a interface with the interlayer insulating film 31 so as to have a vale of c>a>b. In a region corresponded to the LDD region 26-2, the second layer 28b of the gate wiring line layer 28 is processed so as to obtain total thickness of the gate wiring line layer 28 comprised by the first layer 28a and the second layer 28b as 200nm or less. Then, using the gate

insulating wiring line 28 as a mask, the LDD region 26-2, the source region 26-3 and the drain region 26-4 of the semiconductor layer 26 are subjected to a phosphorous (P+) and ion doping simultaneously in a self-aligning manner at a same time under a self-activation condition that 50 KeV as an acceleration voltage and 5E16/c㎡ as a carrier concentration .

[0023]

⑤ As shown in Fig. 3 (e), the interlayer insulating film 31 is formed.

[0024]

⑥ As shown in Fig. 3 (f), contact holes 33a and 34a are formed.

[0025]

⑦ As shown in Fig. 3 (g), a source electrode 31 and a drain electrode 32 are formed and complete a TFT 16.

[0026]

Therefore, as for the manufacturing process ④, in a region where a gate wiring line layer of MoW is processed to have a thickness of 200nm or less with a doping under an accelerating voltage of 50KeV, phosphorous (P+) ion is applied into the LDD region 26-2 of the semiconductor layer 26,

and by one time ion doping, the LDD region 26-2, the source region 26-3 and the drain region 26-4 are automatically formed because the ion that penetrate the gate wiring line layer 28.

[0027]

In measuring a hundred points of an in-plain variation in a mobility and a threshold voltage of the TFT 17 formed in such manufacturing process, a stable characteristic with a very high mobility and very small variation in a mobility and a threshold voltage, comparing to the wide variation in the mobility and a threshold of forgoing TFT, is obtained. existing TFT's mobility is 20 to 100c㎡/Vs, and its threshold voltage is 1 to 6V, on the other hand, TFT 17' s mobility is 110 to 130c㎡/Vs and its threshold voltage is 2 to 4V. Under TFT 17's conditions of a gate-source 0V bias and its drain-gate 20V bias, 90℃ and 1000 seconds, a vicinity mobility and a threshold voltage are compared in a Bias Temperature Stress (hereafter abbreviated as BTS) test. In measuring a hundred points, a shift in mobility and a threshold voltage are not shown. Also, as for a crystal display device 16, a hidden portion is not shown and a display image with good quality is obtained.

[0028]

By structuring as this, forming the corresponding portion to the desired LDD region of the first layer 28a and the second layer 28b in the gate wiring line 28 into forwardly and inversely tapered respectively, conducting ion doping to the LDD region 26-2, the source region 26-3 and the drain region 26-4 simultaneously with one time of doping in a self-aligning manner without using a resist mask by decreasing the doping concentration of phosphorous (P+) ion at a tapered portion in a doping process, and decreasing the number of a process are possible. With this, compared to existing one, a LDD length can be controlled more precisely and obtained easily without producing a dispersion of an LDD length by a doubling gap of a resist mask, a dispersion of an amount of side etching of a gate wiring line layer, which previously occurred. In addition, the TFT 17 with high mobility, and a characteristic with small variation in mobility and a threshold voltage are obtained. Thus the crystal display device 16 using TFT with high mobility and a stable characteristic can obtained good visual display without a hidden portion in a display, and application to a large type active matrix crystal display device is possible.

[0029]

The LDD length can be controlled easier by setting the gate wiring line layer 28 to a two-layer structure and tapering the first layer 28a and the second layer 28b.

[0030]

Present invention is not limited to the embodiment modes above, and if the theme is not changed, the change is possible. For instance, the angle of tapering is not limited, and controlling is possible in a range of 20 to 50° both in forward and inverse tapering from an experiment. In addition, a gap (c−a) between a wiring line width a in an interface with a first gate insulating film layer of a gate wiring line layer and a wiring line width c in an interface with a second interlayer insulating film is determined arbitrary. However, if (c−a) becomes longer than 2 $\mu$m, TFT mobility becomes smaller, and the workability becomes worse. On the other hand, in a BTS test under conditions of 0V gate-source bias, 20v drain-source bias, 90℃ and 10000 seconds, 0.2 $\mu \leqq (a-b) \geqq 2\ \mu$m is more preferable because shift of a threshold voltage is not occurred if (c−a) is 0.2 $\mu$m or more as Fig. 4 shows.

[0031]

Although thickness of the first and second layers of the gate wiring line layer is in a range that is possible to block ion from penetrating into a channel region, the thickness is to be small as much as possible. However, it is determined in accordance with the value (c − a) set by TFT characteristic. For example, in the case of using MoW as a material for an electrode of a gate wiring line layer and forming by a dry etching employs fluorosis (F), it is preferable to set the thickness of the first layer

to 50nm and set the thickness of the second layer to 350nm to realize that value (c−a) is 1.2$\mu$m, in etching under a condition of tapering angle as 30° . In general, the first layer is thinned down, and the LDD length becomes too short when the thickness gap between the first and the second layers is no more than 200nm. Since it is difficult to coat the inverse tapered portion when the thickness gap is 500nm and more, it is preferable to set the gap thickness to 200 to 500nm.

[0032]

Also, a self-activation conditions when ion doping is conducted to a semiconductor layer is arbitrary determined in a range that ion can penetrate through the tapered portion of the gate wiring line layer so as to the LDD region and the source drain region is formed simultaneously.

[0033]

[Effect of the Invention]

As described above, according to present invention, in the top gate type TFT, by tapering the first layer of the two-structure gate wiring line layer forwardly and tapering the second layer inversely, the LDD region and the source drain region can be simultaneously doped in a self-aligning manner on a semiconductor layer by one time of doping without using the resist mask, and consequently, the number of the manufacturing processes

can be reduced. In addition, without the variation in the LDD length are occurred, more precise control on the LDD length are possible, and the desired length and the TFT with stable characteristic are obtained easily without the decline and the variation in the mobility and the variation in the threshold voltage compared to the existing one. Further, like this manner, by using TFT with high mobility and stable characteristic as the driving element, good visual quality in a crystal display device can be obtained, and application to a larger type active matrix crystal display device is possible.

[Brief Description of the Drawings]

[Fig. 1] A cross-section drawing showing the crystal display device of the embodiment mode of present invention

[Fig.2] A cross-section drawing showing the TFT of the embodiment of present invention

[Fig.3] Drawings showing the manufacturing process of the TFT of embodiment of present invention: Fig. (a) showing a crystallization of its amorphous silicon film; Fig. (b) showing a pattering of a poly silicon film; Fig. (c) showing an formation of a first layer; Fig. (d) showing an ion doping that employs a gate wiring line layer after a tapering; Fig. (e) showing a formation of an interlayer insulating film; Fig. (f) showing a formation of a contact hole; Fig. (g) showing a formation of a source electrode and a drain electrode

[Fig.4] A graph showing an amount of shift of threshold voltage corresponding to the value (c−a) of a gate wiring line layer of a TFT by present invention

[Fig.5] A drawing showing a manufacturing process of existing TFT: (a) showing a pattering of its poly silicon film; (b) showing a formation of an LDD region; (c) showing a formation of a source drain region

[Description of the Codes]

| | |
|---|---|
| 16 | A crystal display device |
| 17 | A TFT |
| 18 | An array substrate |
| 19 | A counter substrate |
| 21 | A crystalline composition of matter |
| 26 | A semiconductor layer |
| 26-1 | A channel region |
| 26-2 | An LDD region |
| 26-3 | A source region |
| 26-4 | A drain region |
| 28 | A gate-wiring line layer |
| 28a | A first layer |

| | |
|---|---|
| 28b | A second layer |
| 32 | A pixel electrode |
| 33 | A drain electrode |
| 34 | A source electrode |